Wax

THE ALOHA SYSTEM	Project: TCU Modem	CCG/G-42	34 pages
Title: DESIGN DESCRIPTION OF THE TCU MODEM		General Document May 14, 1974	
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1. Background

The ALOHA TCU Modem converts sequences of binary digits into signal waveforms suitable for transmission over FM radio channels. It also accepts similar waveforms and converts them back into received bit sequences. The modulation method selected for the TCU modem is Differential-Binary-Phase-Shift-Keying (DBPSK) of a carrier signal which has a frequency equal to the bit rate. This modulated carrier is in turn used to modulate an FM radio transmitter, and is also recovered from the output of an FM receiver. Thus the overall data modulation system is actually FM/DBPSK, where the DBPSK carrier is actually a sub-carrier of the FM radio carrier. Although this approach is wasteful of bandwidth, it will be shown to have some practical advantages over a straightforward FSK radio carrier modulation approach.

The primary design constraint of this system is the need to use commercially-available low-cost radios in order to implement data terminals for system quickly and with minimum cost. At the assigned frequencies of THE ALOHA SYSTEM (407.350 and 413.475 MHZ) the types of radios which are most readily available are FM radio transceivers used for mobile radio communications systems. These radios typically use phase modulators to synthetically produce frequency modulation. FM detection is performed by means of a discriminator circuit. Therefore, true FM cannot be produced unless the transmitter's modulator circuit is modified to respond to the d.c. component of the binary data signal. In the receiver, accurate recovery of this d.c. com-

ponent can be a considerable problem due to drift in discriminator characteristics. Also, combined frequency instability of the receiver's local oscillator and the transmitter's carrier oscillator can cause large d.c. offsets.

The receiver problems could be alleviated by the use of high-stability crystal oscillators and crystal discriminators, but such modifications would be expensive and time-consuming. The alternative is to use A.C. coupling out of the discriminator followed by a d.c. restoration circuit. D.C. restoration can present some formidable circuit design problems, requiring tradeoffs between d.c. response time and the maximum length of continuous ones or zeroes allowable in a data sequence. The maximum length of continuous ones or zeroes also effects the design of the bit timing recovery circuit, which is usually a phase-locked-loop. The requirements of rapid bit-timing acquisition at the initiation of a data packet and slow response to long sequences of ones and zeroes are contradictory and require some sort of design compromise. One possibility is to "scramble" the data by encoding it with a pseudo-random bit sequence, thus providing a low probability of long strings of ones or zeroes. A decoder at the receiving modem is required to recover the source data and must be synchronized at the beginning of each data packet.

An alternative to encoding the data with a scrambler is to modulate a sub-carrier with the data. A sub-carrier operating at a frequency equal to the bit rate can be phase modulated by the data so that a power spectrum is produced which is concentrated near the bit rate frequency and contains no d.c. component. Thus the d.c. recovery problem no longer exists for this type of modulation, at the expense of greater required bandwidth in the FM receiver.

The modulated sub-carrier is the signal actually used to modulate the FM transmitter. Since it contains no d.c. component, it is well suited as a source to the transmitter's phase modulator. Thus, the sub-carrier approach has been adopted as a convenient method of modulating standard FM transmitters and recovering the signal from standard FM receiver discriminators.

Since the signal power of the modulated sub-carrier is concentrated near f_c (where f_c is the sub-carrier frequency), a phase-locked-loop (used for bit-timing recovery) is readily kept in phase with the received data signal. Investigation of the bi-phase modulated sub-carrier spectrum, Fig. 1, shows that the low frequencies roll off at the rate of 6 dB/octave (Gaussian-distributed random bit sequence assumed). Thus a single low-frequency d.c. de-coupling time constant can be used to match the low-frequency spectral response of the receiver to that of the data signal and also provide d.c. isolation. This time-constant allows d.c. isolation between the modem input and the discriminator output and yet ensures that the majority of the d.c. offset due to discriminator unbalance, radio frequency errors, etc., will decay out rapidly after the RF carrier appears at the receiver. Although this response time is not critical to the transient response of the TCU modem, which has an input carrier present at all times, it is very important to reliable data packet acquisition for the MENEHUNE modem and other Fast Sync modems used in remote TCU's which operate off of the packet repeater.

One other FM-radio-oriented problem needs discussion before we turn our attention to the modem design problems. This is the need for pre-emphasis and de-emphasis in FM radios using discriminator-type FM detectors. As is

well known, the noise power density spectrum at the output of an FM discriminator with weak noise is not flat but is proportional to the square of the modulating signal's bandwidth, for a given maximum frequency deviation. This is shown in Wozencraft and Jacobs[1] to be

$$\overline{n^2(t)} = \frac{1}{3}\left(\frac{W_m}{W_1}\right)^2 \frac{N_0}{2E_s}$$

where W_m = signal bandwidth

W_1 = maximum instantaneous frequency deviation

N_0 = two-sided noise spectral density into the discriminator

E_s = signal energy

This output noise spectrum can be "bleached" (i.e., made flat) by inserting an integrating filter at the discriminator output. This "de-emphasis" filter will distort the signal spectrum unless a compensating "pre-emphasis" filter is used in the transmitter, prior to the frequency modulator. The use of pre-emphasis and de-emphasis filters in the FM radios ensures an output signal in white Gaussian noise, under the conditions of weak noise. Under stronger noise conditions, threshold effects take precedence and the noise assumes an impulsive characteristic. These impulse anomalies have been studied by Rice[2] and are discussed in Wozencraft and Jacobs.[3] This impulse noise causes the channel to degrade rapidly below the threshold signal-to-noise ratio of the FM receiver. This sharp threshold characteristic of FM receivers can be a great disadvantage, particularly when the received signal strength is fluctuating

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[1] Wozencraft, J. M. and Jacobs, I. M., "Principles of Communication Engineering," pp. 651-654, Wiley, New York, 1965.

[2] Rice, S. O., "Noise in FM REceivers," Chapter 25 of Proceedings of the Symposium on Time Series Analysis, M. Rosenblatt (ed.), Wiley, New York, 1963.

[3] Wozencraft, J. M. and Jacobs, I. M., "Principles of Communication Engineering," pp. 661-664, Wiley, New York, 1965.

at an average level near threshold. This is one of the unfortunate aspects of using FM radios, so that it behooves the system designer to ensure adequate fade margins are maintained in the various line-of-sight paths of the system. For mobile terminals, these margins cannot be guaranteed, but packet transmission repeating can usually ensure packet throughput when signal strength is varying randomly at rates which are relatively slow compared to packet duration period. The short-burst and repeat technique is also useful when intermittent interference is encountered.

2. TCU Modem Design

As stated in the previous section, the modem employs differential binary-phase-shift-keying of sinusoidal carrier waveform, which has a frequency equal to the bit rate. The differential-phase-shift keying is used to remove ambiguity from the received carrier phase, and is not used for purposes of comparison detection. The demodulator portion of the modem employs coherent detection, followed by a differential de-coder to recover the data. This approach was adopted since the received carrier input is present at all times at the TCU (the MENEHUNE continuously transmits to all of its KEIKI's). Thus if phase sync is lost for any reason, the TCU modem automatically re-syncs to the incoming phase with no action required on the part of the MENEHUNE, such as sending out sync characters, etc. In order for automatic re-sync to take place, the standby signal condition must be one of continuous phase-reversals per bit. Since the MENEHUNE normally transmits a logic ZERO when no data is being sent, the ZERO condition is encoded into the binary phase reversal per bit condition and the ONE condition is sent as a continuous phase, with no reversal. This differential encoding is not necessary on the channel into the MENEHUNE from the KEIKIs since the burst nature of the transmission allows phase initialization at the beginning of each packet. However, the same coding scheme is used for this channel so as to maintain consistency in the design of the modems. The differential encoding will cause a predominance of double-bit errors to occur, when errors do occur, but this is not a critical problem since only one error is needed to require a packet retransmission and the second error adds little to the packet error rate in the

case of detection-retransmission systems. In the case of forward-error-correction systems the double-bit errors become more important, but they can be handled with appropriate error-correction algorithms since their occurrence is known a priori. However, to simplify error-correction, it would probably be advantageous not to use differential encoding, and this approach is indeed being studied for use in the ATS-1 modem which will be used in conjunction with an error-correction system.

A block diagram of the TCU modem, ALOHA drawing number RF-1012, shows the overall design layout. At the buffer interface are shown seven interchange signals. These are logic-level signals, compatible with 7400-series TTL. The interchange signals are defined as follows:

ϕ_T - Transmit Data Clock

ϕ_R - Receive Data Clock

RS - Request-to-Send Flag

CS - Clear-to-Send Flag

SDA - Transmitted Data

RDA - Received Data

RG - Receive Gate (Carrier On)

The modem supplies both the transmit and receive data clocks to the connected data equipment. The transmit clock is derived directly from a crystal-stabilized clock oscillator and the receive clock is locked to the received data clock rate. The convention used is that data is transferred on the rise of the clock and sampled on the fall of the clock pulse, which is symmetric. CS and RG also change state on the rise of the appropriate clock. RS may be non-synchronous since it is internally clocked in the modem.

Modulator

Referring first to the modulator section, the CS DELAY provides sufficient delay after the transmitter is turned on for the receiving modem at the far end of the link to become synchronized to the incoming data signal. When the CS flag is received by the data equipment, transmit data may then be transferred to the modem. A "high" level on RS, CS or RG constitutes an "ON" condition. For the data signals, a "high" level is a ONE and a low level is a ZERO.

The Data Gate allows transmit data to enter the Differential Encoder when CS goes high. Otherwise, a ZERO condition is maintained into the encoder. The Differential Encoder is a logic circuit which changes state every bit time while a ZERO is present at its input. It remains in steady state when a ONE is present at its input. The output of the Differential Encoder is used to set the phase of the carrier signal in either a 0° or 180° state. This action is performed by a bi-phase (PSK) modulator under control of the Differential Encoder.

Since the signal out of the PSK Modulator has a rectangular time waveform, thus containing harmonics of the carrier fundamental, it is passed through a low-pass filter to suppress all harmonics above the fundamental frequency of the carrier. This is necessary to keep from overmodulating the FM radio transmitter and wasting spectral power. The filtered carrier signal is then applied to an FM pre-emphasis circuit before being sent out to the FM radio transmitter's modulator. In addition to this baseband signal, a Request-to-Send (RS) signal is also shown at the Transceiver Interface. This is simply used to turn on the radio transmitter so as to

establish the link to the remote receiver.

Demodulator

The demodulator is somewhat more complex than the modulator. First, the received baseband signal is de-emphasized (and d.c. de-coupled). It is then low-pass filtered to remove the high-frequency components of the baseband noise signal outside the spectrum of the data signal. It is then amplified and hard-limited before being converted to a TTL signal for digital processing. Since the signal information is contained in the zero-crossings of the data carrier, hard-limiting removes any amplitude information which could degrade the zero-crossing threshold detector decisions (assuming limiter input S/N ratios greater than - 6 DB). Thus only phase-noise is left (hopefully) along with the data signal. The probability density of this phase-noise is well known (for a white Gaussian noise source) and the error probability as a function of signal-to-noise ratio has been calculated, assuming matched filter detection.[5]

The limiter circuit is followed by a circuit called Noisy Clock Recovery Circuit. This circuit uses a set of monostable multivibrators (one-shots) to frequency-double the signal, divide back to the clock rate, and wide band filter it to produce a clock signal which still contains a large noise component but no modulation components. This noisy clock is then fed to a narrow-band Digital Phase-locked-loop Clock Recovery Circuit which removes most of the noise and produces a clock signal with very little jitter, which is phase-locked to the incoming data signal. The narrow bandwidth

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5 Lucky, R. W., Salz, J., and Weldon, E. J., Jr., "Principles of Data Communication," pp. 248-251, McGraw-Hill, New York, 1966.

4 Gardner, F.M., "Phaselock Techniques," pp. 55-58, John Wiley & Sons, New York, 1966.

of the loop (2 Hertz) precludes rapid acquisition and is designed for lock-up on a continuous signal. The one-second time-constant of the loop causes the recovered clock phase to be relatively unperturbed by any noise burst or short-period loss of signal.

The smoothed clock signal is then fed to several points in the demodulator for additional processing of the data signal. First, it is fed to the PSK Demodulator which removes the binary phase modulation from the signal. The resultant differentially-encoded data signal, which is still noisy, is then fed to the matched filter which is the Digital Integrate and Dump Filter. The smoothed clock is used with this filter to interrogate the output of the integrator and reset it every bit interval, T. Finally, the smoothed clock is used to sample and shift the Differential Decoder register every bit interval so that the resultant received binary data signal is made available to the data terminal equipment.

An additional phase detector in the S/N Threshold Detector is used to compare the phase of the recovered clock to that of the noisy clock. When the smoothed clock is properly locked-onto the data signal and in phase with it, a maximum d.c. level will result from the phase detector which, with the Integrator, acts as a correlation detector. The d.c. level out of the Integrator is a direct function of the phase relationship between the input signal and the recovered clock and also of the signal-to-noise ratio. Thus, it detects not only how well the demodulator has locked onto the signal but also how noisy is the signal. By feeding this d.c. signal into a variable threshold detector, the modem can be adjusted to accept a data signal at a specified signal-to-noise ratio. Thus, the Threshold Detector

has as its threshold reference a level termed S/N Threshold Reference. The output of this circuit is the Receive Gate (Carrier Sense) signal. In the Fast Acquisition version of the modem the S/N Threshold Detector is used principally as a burst acquisition detector and the threshold adjustment is used to set the false-alarm-rate of the modem. In the TCU modem the Integrator time constant is set to provide a very small variance about the average d.c. level. It has a response time equal to that of the loop.

3. Detailed Circuit Description

Details of the circuit design are provided in the attached ALOHA drawing number RF 1013. The circuitry will be discussed by sub-system and drawing page number. Signal timing relationships are shown in figures 2 and 3 and are keyed to drawing RF 1013.

Modulator Sub-System (RF 1013-01)

At the top of the drawing is shown the crystal clock oscillator and its divider string. Since the modem is designed for operation at either 9.6 kB/s or 24 kB/s, two different clock frequencies are used. The 9.6 kB/s version is presently implemented. This version uses a 9.8304 MHZ crystal oscillator, the output of which is fed to an SN 72710 comparator for shaping into TTL levels. The 74H73 dual flip-flop I.C. divides this frequency down to 2.4576 MHZ, which is used for the high speed clocks, CO and CE, in the modem. The two SN7493 four-stage ripple counters divide down from the high speed clock frequency by a factor of 2^8 to provide the transmit clock, β_T. This clock is also used for modulator functions.

The request-to-send signal SR is filtered by R11 and C5 and used to gate ON the SN74121 which provided the CS time out delay. SR is also routed out to the radio transmitter through a buffer. At the end of the CS delay period, the first flip-flop of the SN74107 is toggled to produce a ONE at the Q output. This state is aligned with the rise of β_T by the second flip-flop and fed into the SN7413 Schmitt Trigger data gate to allow data to enter the modulator. R34 and C8 are used to filter the data signal and provide a small delay to ensure proper clocking through the SN7400 gate. The data signal is used to control toggling of the SN74107

flip-flop to provide the differentially-encoded data signal into the Biphase Modulator. The flip-flop then steers either the ϕ or $\bar{\phi}$ signal to the transmitter sub-system, providing a differentially-encoded bi-phase-shift-keyed signal. The timing waveforms are shown in Figure 2.

XMTR-RCVR Sub-System (RF 1013-02)

The top part of the drawing shows the transmitter circuits. Capacitive coupling is used into the AC Amplifier to remove the d.c. component of the TTL data signal. The amplifier reduces the signal amplitude for processing in the four-pole low-pass active filter. There are two poles per filter stage, each of which uses an SN 72741 operational amplifier as its active element. Each filter stage is designed to have a maximally-flat (Butterworth) filter characteristic. The corner frequency of each filter section is set at twice the clock frequency to ensure minimal phase shift of the modulation spectral components and yet keep the spectral levels of higher harmonics at least 20 dB below the fundamental signal spectral level. Phase-linear filters could have been used, but investigation of these filters indicated little advantage over the simpler Butterworth filters for this application. Thus, no strong harmonics are contained in the filtered data signal which would cause overmodulation of the FM radio transmitter. The filtered waveform is shown in Figure 2.

The pre-emphasis filter follows the low-pass filter. The response of this filter is designed for use with the phase modulator of the FM transmitter. The pre-emphasis time constant was selected experimentally by optimization of the data signal eye pattern at the MENEHUNE receiver when transmitting a continuous pseudo-random data sequence from a TCU radio

transmitter and modem.

Examining the receiver circuits, we find the de-emphasis filter first in the signal-processing chain. This circuit is designed to have a 75 microsecond time-constant, the same as that used in the MENEHUNE's receiver. This is a standard time-constant, being an acceptable compromise between a true integrator and a close approximation to true integration for a bandwidth of 10 KHZ. A d.c. zero adjustment is provided at this stage so that clipping will take place symmetrically in the First Limiter stage (all stages are d.c. coupled up to the Second Limiter). Again we have a four-pole low-pass filter (maximally flat). This filter removes high frequency noise components from the discriminator output without distorting the data signal (f_c = twice the bit rate).

The First Limiter has adequate gain to provide hard limiting of the data signal. In fact, this circuit will hard-limit on noise, when no signal is present. The Second Limiter is basically a threshold level detector which converts the data and noise signals to TTL levels for digital processing. An SN72810 high gain comparator is used for this purpose. The a.c. coupling isolates this comparator from any d.c. drift in the preceding stages. The SN7404 inverter is used as a buffer amplifier to the remainder of the demodulator circuits. The filtered and limited waveforms are shown in Figure 3.

Clock Recovery Sub-System (MP 1013-03)

This sub-system is composed of two main circuits: the Noisy Clock Recovery Circuit and the Digital Phase-Locked-Loop Clock Recovery Circuit (DPLL).

The Noisy Clock Recovery Circuit is made up of four one-shot multivibrators, as shown in the left part of the drawing. The first two one-shots are contained on the SN 74123 I.C. These are short-pulse (200 ns) one shots which are respectively triggered by the rise or fall of the received signal. Either of these two one-shots will trigger a third one-shot and thus act as the equivalent to a frequency doubler. However, instead of triggering a one-shot with a time duration of one-fourth the bit interval, which would cause a twice-rate clock to be produced, the third one-shot is set for a time duration of approximately three-fourths the bit interval. It thus acts to filter out the twice frequency component but will still respond to either phase of the signal, whichever triggered it first. The fourth one-shot is triggered by the third one-shot and has a nominal duration of one-half the bit interval. This duration can be adjusted by means of R32 to produce a symmetrical clock signal. When ZERO bits are received the data signal appears as a half-rate clock signal and thus causes the noisy clock circuit to lock to the data signal phase in a fixed phase relationship. However, receipt of ONE bits causes the data signal to appear as a clock signal. The noisy clock circuit can arbitrarily lock either in phase or 180 degrees out of phase with this signal. Under the condition of only ONES being received, missing an odd number of zero crossings, after having initially acquired phase, would cause slippage to the opposite phase and inversion of the recovered data. The appearance of a single ZERO will re-establish the initial phase, if it had been initially established by a ZERO signal. Therefore ZERO's are always initially sent in the packet preamble to set the initial phase reference. In the case of

the continuously received signal at a TCU, ZERO's are always received between packets. The response time of the phase-locked-loop clock recovery circuit is much greater than the expected period of the longest sequence of ONE's in a packet so that the probability of a phase change during a packet interval is very small. In the Fast Sync modem, this probability is larger since its loop has a faster response than the TCU modem's loop, but is still small enough not to be considered a serious problem.

The Noisy Clock signal is fed to the phase comparator of the DPLL. Here it is compared to a 90 degrees-phase-shifted version of the recovered clock by means of an SN 7486 Exclusive OR circuit. The output of the SN 7486 is inverted and referenced to the regulated +5 volt power supply via an SN 7403 open-collector NAND circuit and clamping diode. The switching output of this circuit, which has an average d.c. level associated with its average ON-OFF ratio, is integrated by a simple low-pass filter, R36 and C22. The resultant average d.c. signal is then presented to two threshold detectors consisting of SN 72810 comparators. These comparators put out enabling signals to a pair of 3-input SN 7410 NAND gates as shown in the drawing. One of the two gates will be enabled whenever the threshold of its associated comparator is exceeded (high or low thresholds). The threshold voltages are set symmetrically on either side of the phase comparator output voltage representing the in-phase condition. The transfer function of the phase comparator is shown in Figure 4.

For stable loop conditions, the loop locks up with a phase difference between 0 and π radians, servoing about the π/2 point. Thus the high and low threshold voltages are set on each side of the +2.4 volt level. The loop operates as a "Bang-Bang" servo as shown in the following description. If the high threshold is exceeded a high frequency pulse is gated into the SN 74123 dual one-shot, causing it to fire in sequence. The first one-shot delays the output of the second one-shot which is a short pulse. This pulse is inserted at its associated SN 74H00 NAND gate so as to increase the count by one into the six-stage counter made up from two SN 7493 ripple counters. If the low threshold is exceeded, the SN 74121 one-shot is triggered. It puts out a pulse long enough to delete a counter input pulse by means of its appropriate SN 74H00 NAND gate. Thus the clock rate appearing at the output of the counter string can be increased or decreased incrementally, resulting in a variable frequency oscillator running off of the modem's high speed crystal clock. The rate at which the clock frequency can be incremented is controlled by the other SN 74121 one-shot shown in the DWG. Whenever either the increment or decrement one-shot is fired, the SN 74121 one-shot is triggered to put out an inhibit pulse to the two three-input SN 7410 NAND gates. This prevents any further frequency adjustment during the period of the one-shot and thus effectively controls the rate at which the loop can servo. Thus, capacitor C23 is used to set the bandwidth of the loop. Since a six-stage counter is used, the recovered clock phase can be incremented in 2^6 steps providing a phase resolution of 5.6 degrees. Thus the high and low thresholds should be set to about ±0.2 volts about the zero error point to return the loop to the center of its range

(0.175 volt is equivalent to 5.6 degrees). In practice the thresholds are set close enough to minimize the dead zone but far enough apart to prevent excessive hunting of the loop (in order to minimize clock jittar).

The 90 degree phase shift of the recovered clock is obtained by means of the J and K steering inputs of the SN 74107 flip-flop shown. Toggling this flip-flop with a twice-rate clock signal provides the one-fourth clock period shift. This phase shift is necessary since the loop locks 90 degrees out of phase with the noisy clock. Timing waveforms are shown in Figure 3.

Demodulator Sub-System (RF 1013-04)

The demodulator sub-system is composed of three functional circuit groups. These are the PSK (or bi-phase) Demodulator, the Digital Integrate And Dump Filter, and the Differential Decoder.

The PSK Demodulator is simply an Exclusive OR, SN 7486, which compares the recovered clock synchronously to the received data signal. The resultant output is the differentially-encoded data signal with noise.

This signal is fed into the Integrate And Dump Filter, which is the matched filter for a binary waveform with signal element duration T. This filter is designed to simply estimate, during the bit interval, whether the demodulated signal is at a high or low level for more than half the bit interval. A digital integrator is implemented by means of an eight-stage counter driven by the modem's high-speed clock. Hard decisions are made by determining if the count is greater or less than a count of 128 (out of a total count of 256 per bit interval). This is the equally-likely threshold level. The counter is enabled by the high state of the demodulated signal.

A noiseless signal would allow a full count of 256 during the bit interval for a high state. The count would be zero for a low state input. Thus, noise impulses changing the actual state up to half the bit interval will be filtered out. The counter uses a pair of SN 74161 synchronous binary counters. A flip-flop from an SN 7407 I.C. is used to synchronize the enabling signal to the high-speed clock. The half-bit-period count of 128 is decoded by the SN 7430 NAND gate. When the count threshold is detected by this gate, it presets the SN 7472 flip-flop to a ONE out of the Q output. The $\overline{Q}$ output, which goes to a ZERO, is fed back to the SN 7403 NAND gate to turn off further inputs to the counter. As can be seen in the timing diagram, Figure 3, the demodulated ZERO signal is a half-period-shifted replica of the input signal. To maintain alignment with this signal, the integrator is dumped on the fall of the recovered clock. Thus, the inverted clock $\overline{\phi}_R$ first samples the Q output of the SN 7472 flip-flop on the fall of the clock ϕ_R, by loading into the first SN 7474 flip-flop shown on the right of the drawing (D-input is pin HB10). At the same time, the SN 74123 one-shot shown in upper-right is triggered. This one-shot puts out a 200 msec negative-going pulse which resets the SN 74161 counters to the zero count state and resets the Q output of the SN 7472 flip-flop to ZERO. The integrator is thus initialized for the next bit interval.

The third functional circuit group in the demodulator is the Differential Decoder. This circuit operates by storing the previous bit state in a flip-flop and comparing it to the current bit state. This function is performed by two SN 7474 flip-flops, an SN 7486 Exclusive OR gate, and the SN 74123 one-shot, all shown as a circuit group over the label DIFF.DECODER. The one-shot produces sampling pulses occuring on the rise of the recovered clock,

ϕ_R, which shift the one-bit storage register. The output of the Exclusive OR gate is first sampled by ϕ_R by loading this output into the left-most flip-flop. Thus the decoded data signal is shifted out to the data gate on the rise of the receive clock. Shortly after the Exclusive OR gate output is sampled, the middle SN 7474 flip-flop is shifted to prepare for the next bit comparison. The decoder operates simply on the following principle: If the present bit state and the previous bit state are the same, the Exclusive OR has a ZERO output. Since this condition is that a ONE was sent, the inverted output, $\bar{Q}$, of the left-most flip-flop is used to invert the Exclusive OR output. Conversely, if the delayed bit state is different from the present state, the Exclusive OR outputs a ONE which is inverted to a ZERO. This is the condition due to transmission of a ZERO, and is thus decoded as such. Timing waveforms are shown in Figure 3.

S/N Threshold Detector Sub-System (RF 1013-05)

This subsystem is composed mainly of three circuit functions. These are the Phase Detector, Integrator, and Threshold Detector. A Data Gate is also included in this subsystem since it is controlled by the output of the Threshold Detector.

The Phase Detector uses an SN 7486 Exclusive OR gate to compare the phase of the smoothed clock to that of the noisy clock. If only noise is being received the comparator will have an output which is high or low half the time, on the average. This will result in an average output voltage of +2.5 volts. When the DPLL locks onto an incoming signal, the two signals will be in phase agreement resulting in a continuous high output from the SN 7403 NAND gate of almost +5 volts.

The Integrator smooths out the switching waveform to form a continuous d.c. level. The SN 72741 operational amplifier is configured in a follower mode, presenting a high input impedance to the RC integrator to minimize loading. The time constant of the TCU modem's integrator is set at one second, about the same as the response time of the DPLL. This large an integration time makes it relatively insensitive to short periods of signal loss. It also results in a very little fluctuation of the integrated signal due to noise. As the noisy clock signal becomes more noisy, its variance about its mean phase position increases, resulting in the noisy clock signal spectrum widening and its spectral power density level at the zero frequency (d.c.) decreasing. Since the integrator is essentially a narrow band low-pass filter, it puts out a d.c. level proportional to the d.c. component of the phase detector output. Thus the output of the integrator can be used as a direct measure of the signal-to-noise ratio of the received data signal. This output is fed into the next circuit for S/N threshold detection.

The Threshold Detector uses an SN 72741 operational amplifier configured as a schmitt trigger. The output swing of the amplifier is limited to ±5 volts by the two zener diodes CR4 and CR5. Regenerative feedback is employed through resistors R55 and R56 to provide a voltage hysteresis of 0.2 volt. When no signal is detected the voltage appearing at the positive amplifier input is +0.1 volt. The resistance divider R52, R53, and R54 sets the integrator output voltage required to match the +0.1 volt threshold level. When this level is exceeded the threshold detector regeneratively reverts to its other state and the input voltage must then drop to -0.1 volt or

lower to switch it back. The S/N Threshold Adjustment, R54, sets the integrator output level at which the received signal will be accepted. The 0.2 volt hysteresis prevents instability in the threshold detector's output due to small fluctuations in the integrator voltage at threshold. CR6 is used to clamp the output to TTL levels and an SN 7404 inverter is used to invert and buffer the threshold detector output. The output is then fed to an SN 74107 flip-flop where it is aligned with the receive clock so that RG changes state only on the rise of the clock. The $\bar{Q}$ output is fed to the Data Gate to enable the receive data output when RG goes high.

Power Supplies Sub-System (RF 1013-06)

This drawing shows how the various voltages for the modem are derived from a single +5 volt input. A miniaturized d.c.-d.c. converter is used to obtain the ±12 volt power buses for the operational amplifiers and comparators. A 6.8 volt zener diode and emitter follower circuit supplies the -6 volts needed for the comparators.

General Notes (RF 1013-07)

This drawing lists general notes pertinent to the modem components and provides a data rate option table for two different data rates. The modem is presently implemented in the 9.6 kB/s option.

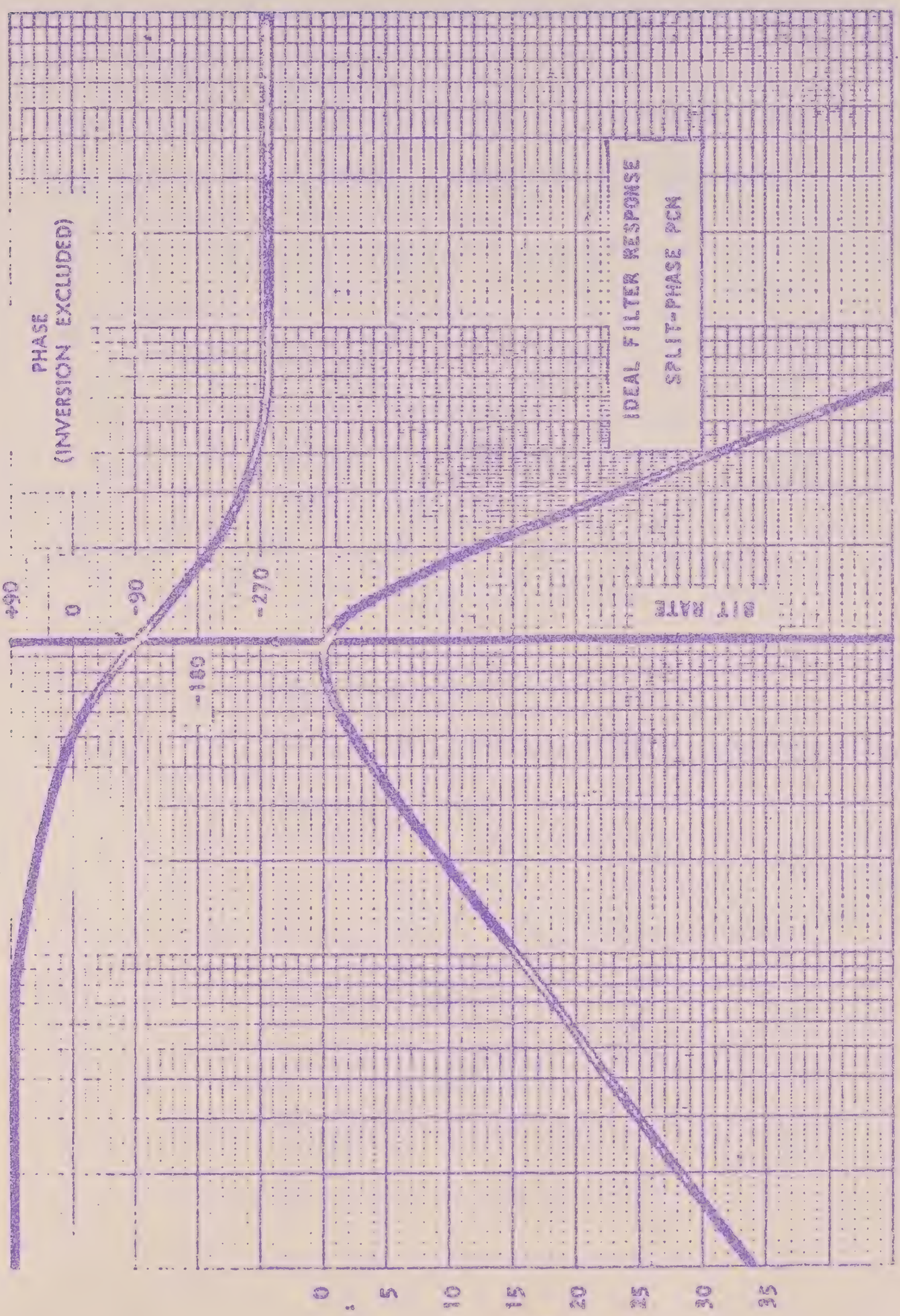
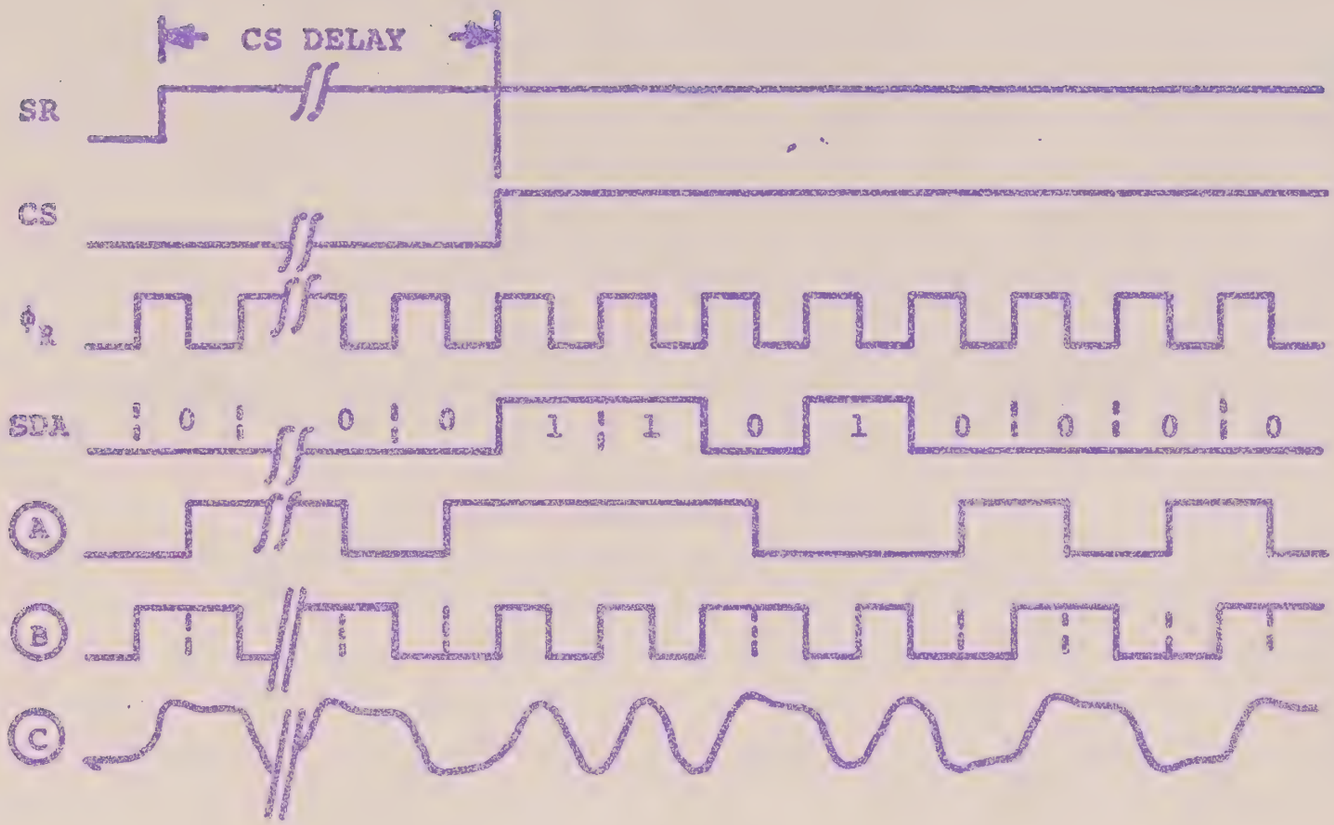


Figure 1 Ideal Filter Response for PCM Bit



(A) - Differentially-Encoded Xmt. Data Signal

(B) - Differentially-Encoded Bi-phase Modulated Carrier

(C) - Filtered DBPSK Carrier

Figure 2

MODULATOR WAVEFORMS

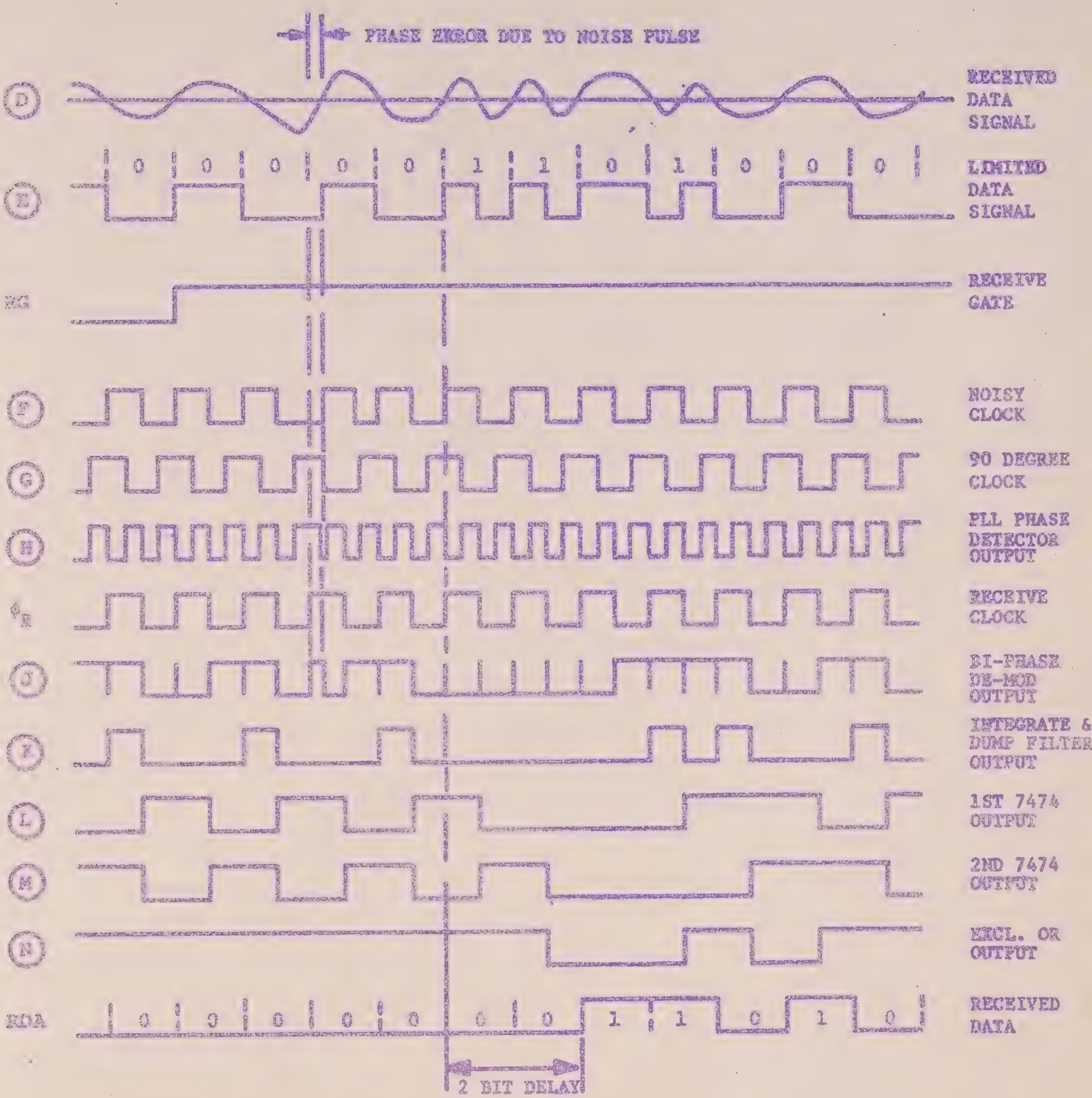


Figure 3

DEMODULATOR WAVEFORMS

T_H : High Threshold

T_L : Low Threshold

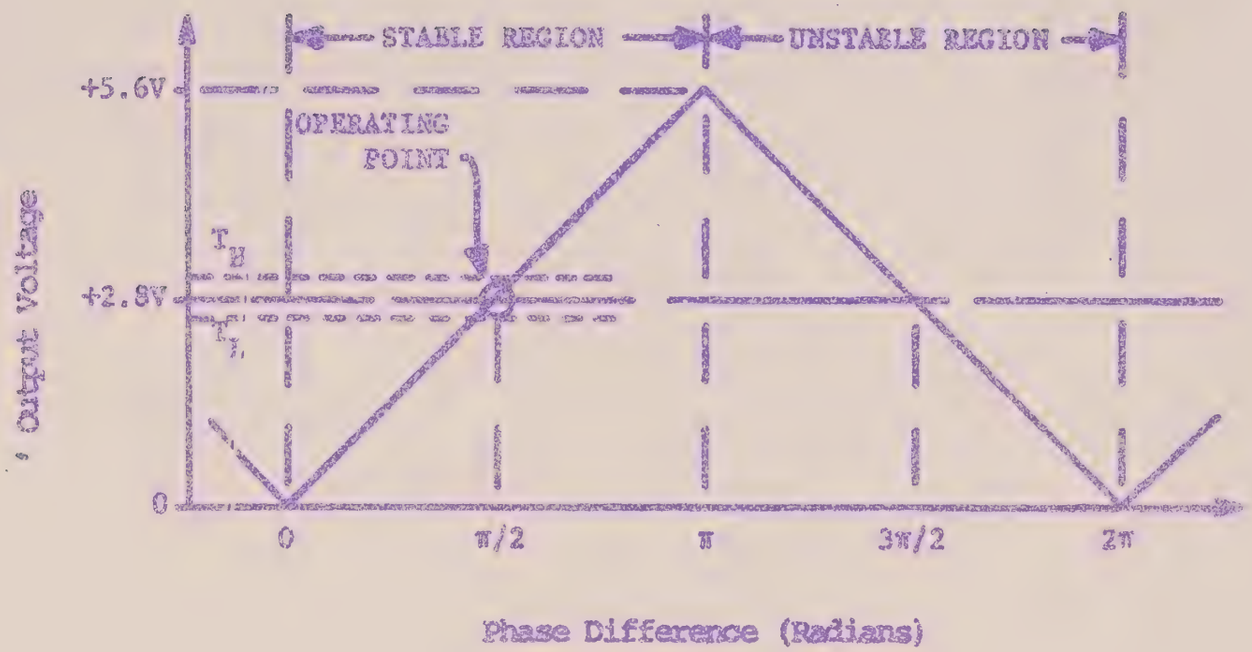
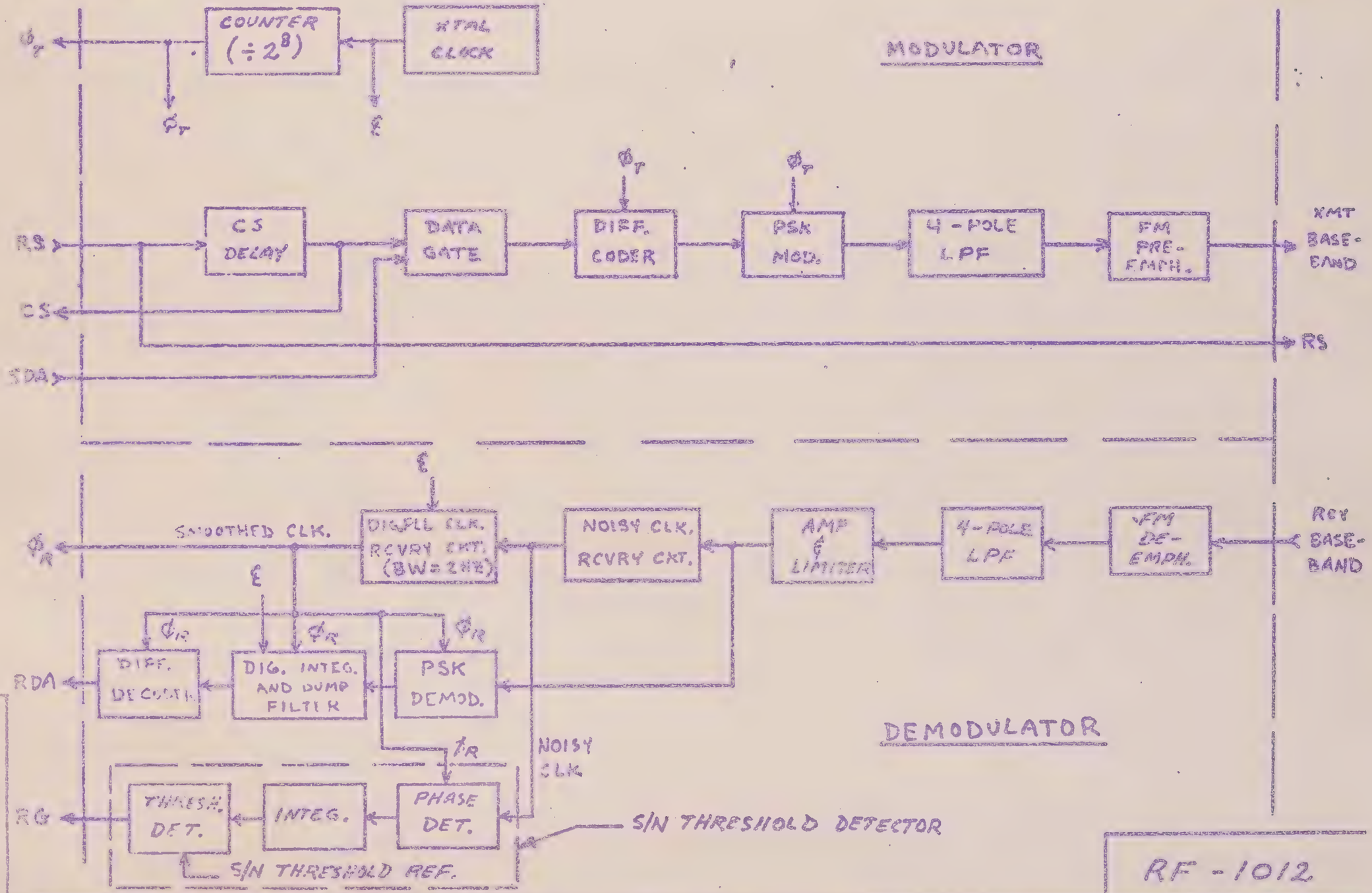


Figure 4

PHASE COMPARATOR TRANSFER FUNCTION

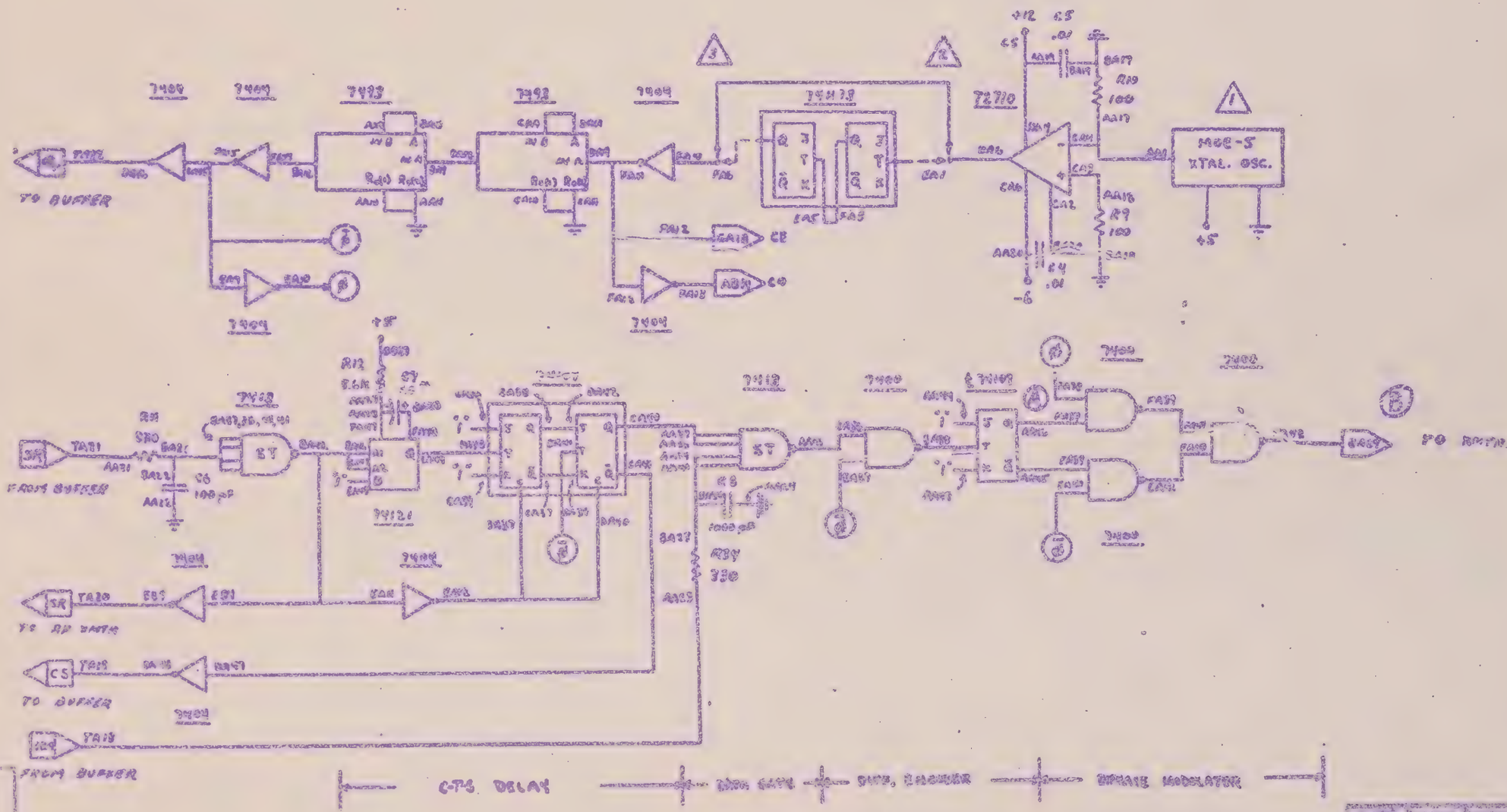
BUFFER INTERFACE

TRANSCEIVER INTERFACE



RF-1012

ALOHA System Project, U. of H.
System TCU Modem Sub-system BLOCK DIAGRAM
Name D. Wax Date 4/2/72
Page 1 of 1



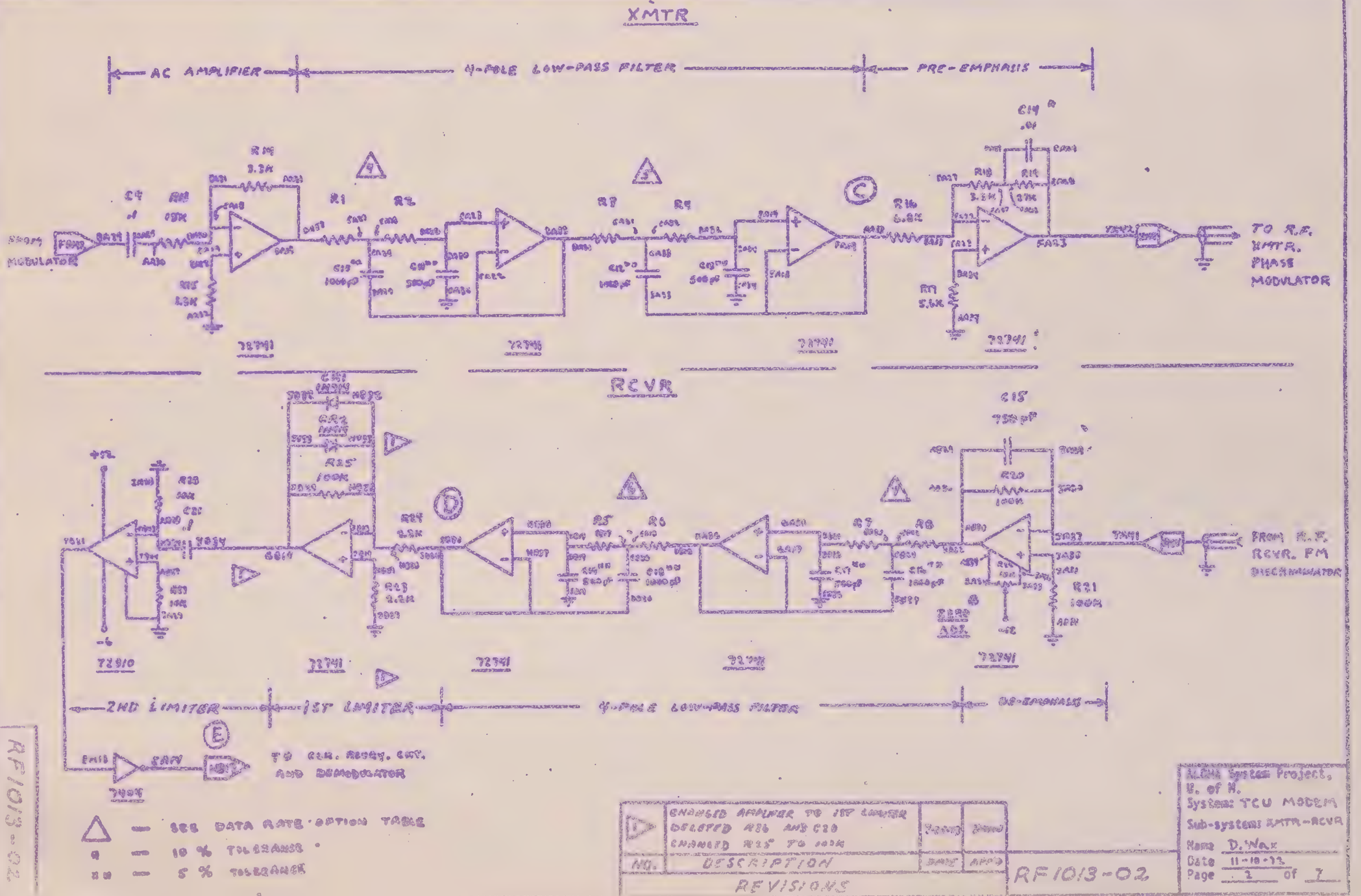
△ — SEE DATA RATE OPTION TABLE

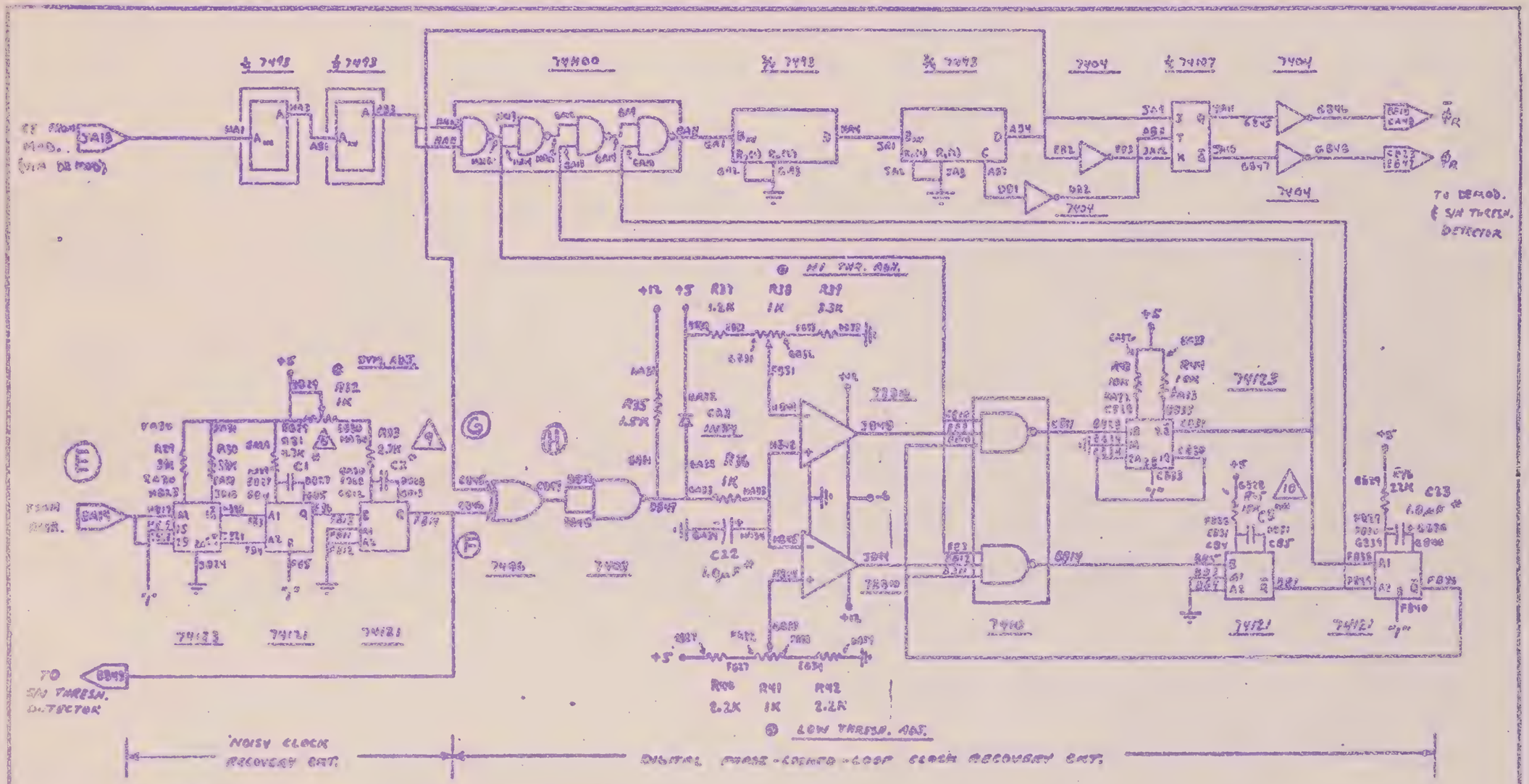
* — 10 % TOLERANCE

RF1013-01

RF1013-01

Name: D. Wu
Date: 11-10-72
Page: 1 of 1


XMTR
AC AMPLIFIER
4-POLE LOW-PASS FILTER
PRE-EMPHASIS
FROM MODULATOR
TO R.F. XMTR. PHASE MODULATOR
RCVR
2ND LIMITER
1ST LIMITER
4-POLE LOW-PASS FILTER
DE-EMPHASIS
FROM R.F. RCVR. FM DISCRIMINATOR
TO R.F. RCVR. AGC AND DEMODULATOR
△ — SEE DATA RATE OPTION TABLE
a — 10 % TOLERANCE
aa — 5 % TOLERANCE
ENGINEER AMPLIFIER TO 1ST LIMITER
DELETED R36 AND C20
CHANGED R35 TO 100K
NO. DESCRIPTION DATE APPD
REVISIONS
RF1013-02
ALOHA System Project,
U. of H.
System: TCU MODEM
Sub-system: XMTR-RCVR
Name D. Wax
Date 11-10-73
Page 1 of 7



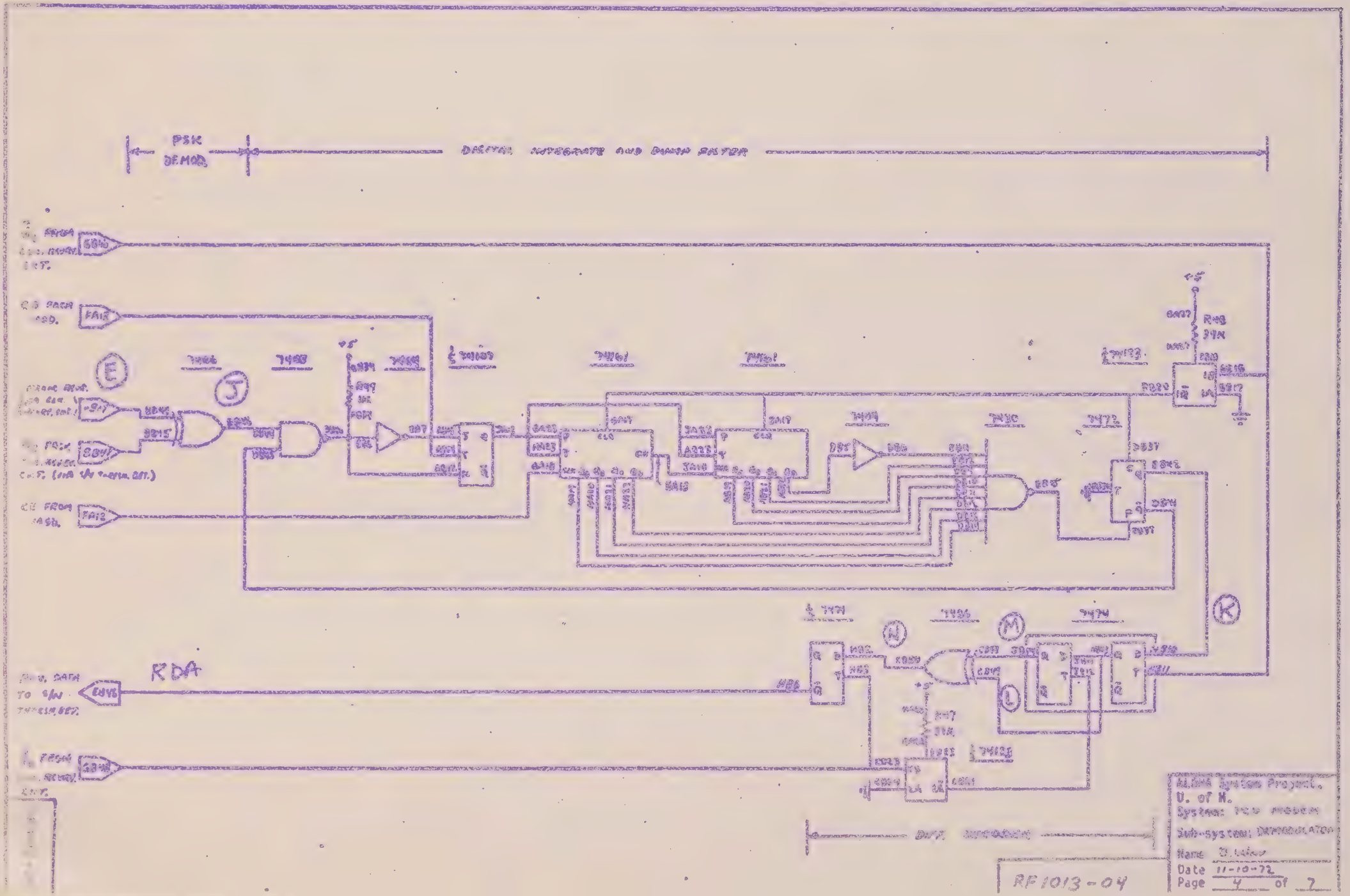
△ — SEE DATA RATE OPTION TABLE

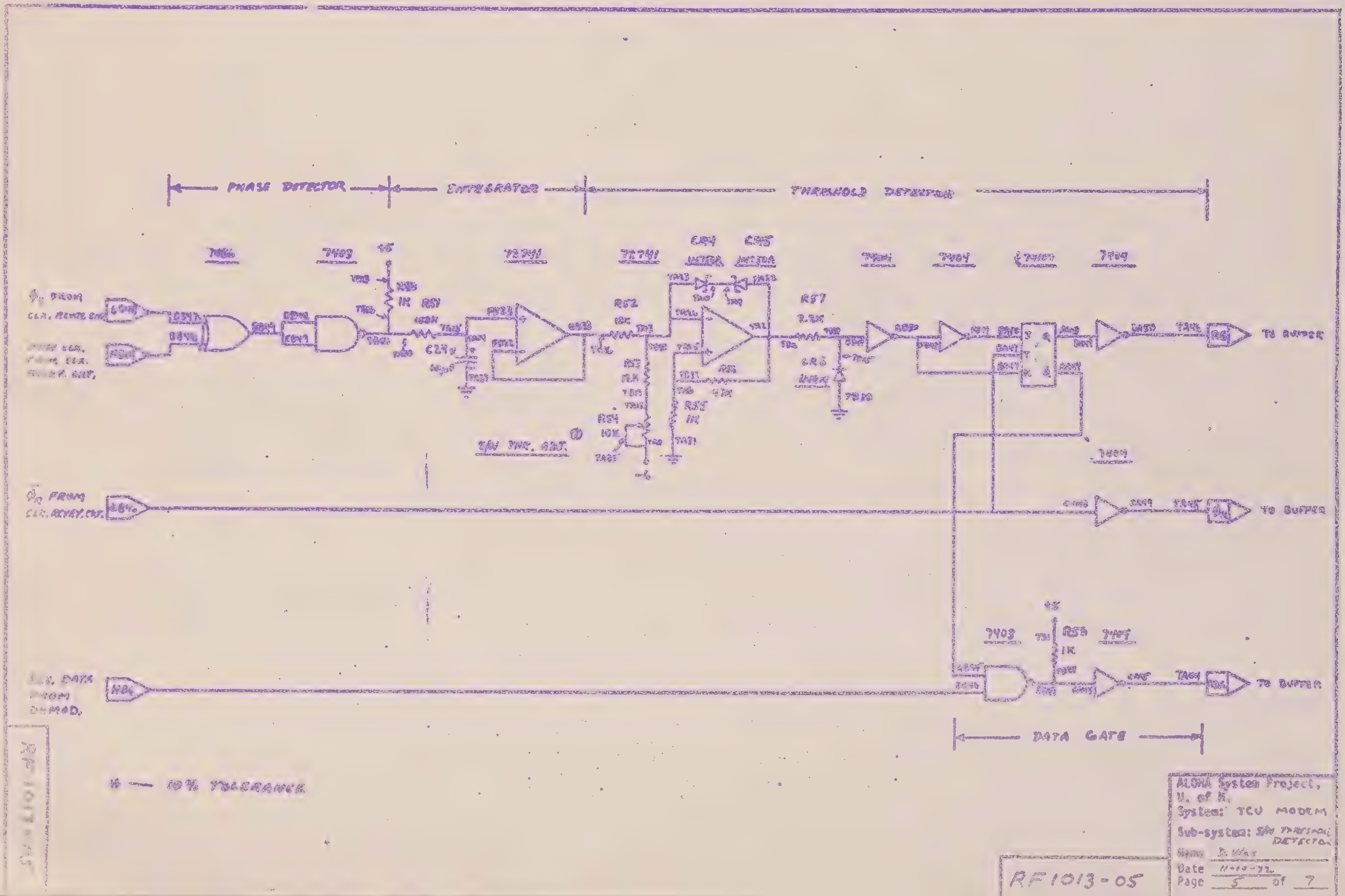
\# — 10 % TOLERANCE

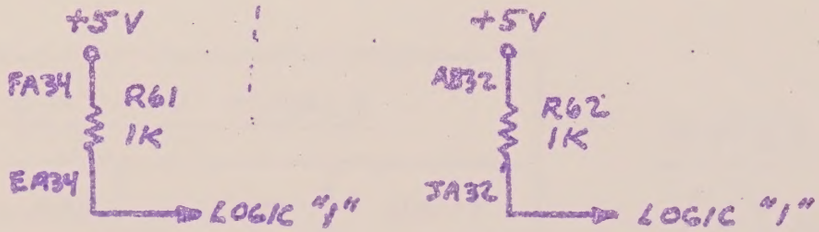
\#\# — 5 % TOLERANCE

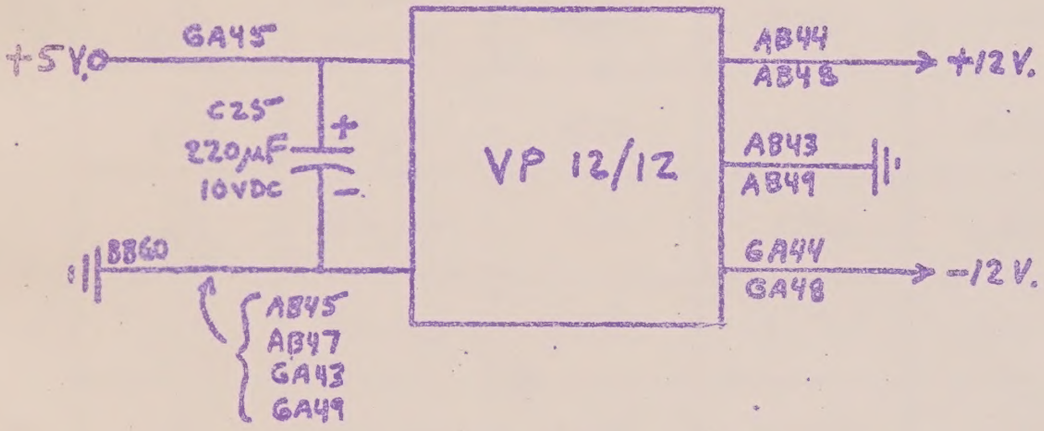
RF 1013-03

M.I.T. System Project, U. of N.
System: TCU MODEM
Sub-system: CLOCK RECVR.
Name D. Way
Date 11-20-72
Page 3 of 7

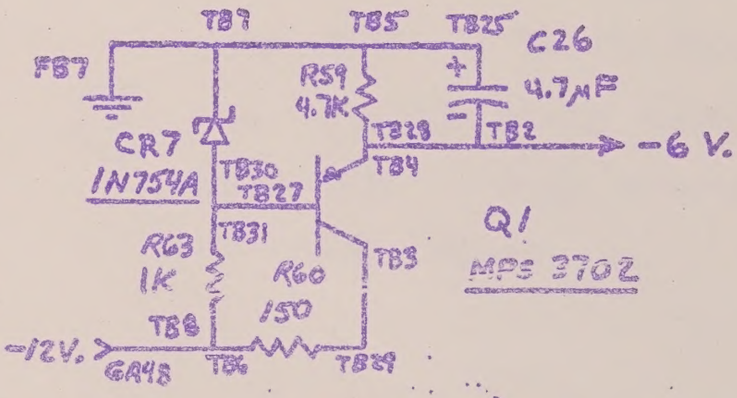

PSK DEMOD.
RDA
RF1013-04
U. of H.
Name
Date 11-10-72
Page 4 of 7


PHASE DETECTOR
INTEGRATOR
THRESHOLD DETECTOR
7486
7403
72741
74107
7404
7409
RS7
2.2K
RS2
10K
RS3
RS4
10K
RS5
1K
RS8
1K
S/N THR. ADJ.
TO BUFFER
DATA GATE
Φ FROM CLK. RCVR. CKT.
ΦR FROM CLK. RCVR. CKT.
RCV. DATA FROM DEMOD.
10% TOLERANCE
ALOHA System Project,
U. of H.
System: TCU MODEM
Sub-system: S/N THRESHOLD DETECTOR
Date 11-10-72
Page 5 of 7
RF1013-05



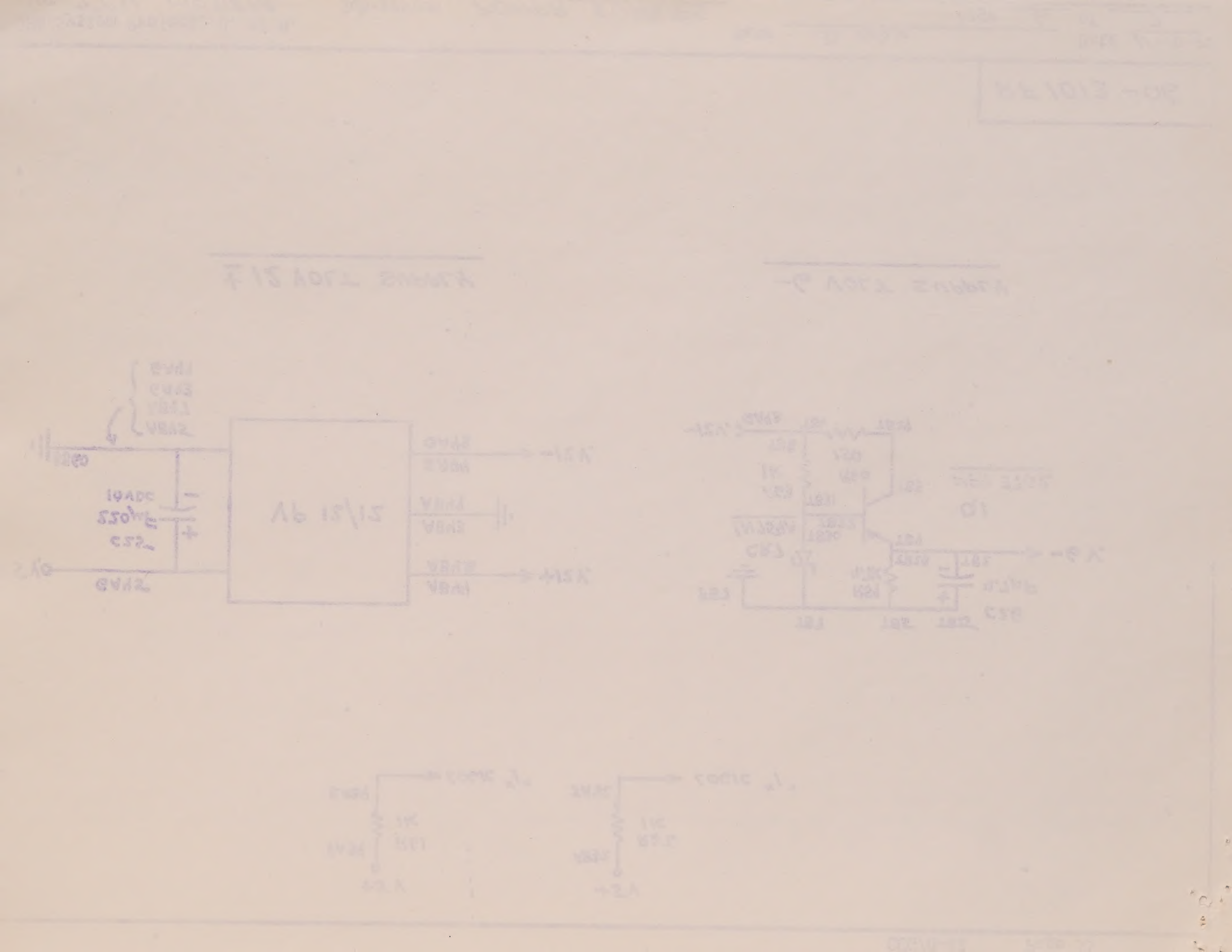


± 12 VOLT SUPPLY



-6 VOLT SUPPLY

RF1013-06



DATA RATE OPTION TABLE

SYMBOL	PARAMETER	9.6 KBS	24 KBS	UNIT
1	FREQUENCY	9.8304	6.1440	MHZ
(3) 2	JUMPER PIN NO.	NONE	EA1	—
(3) 3	JUMPER PIN NO.	NONE	FA6	—
4	R1, R2	10K	4.7K	OHMS
5	R3, R4	10K	4.7K	OHMS
6	R5, R6	10K	4.7K	OHMS
1 7	R7, R8	10K	4.7K	OHMS
8	C1	0.025	0.01	μF
9	C2	0.025	0.01	μF
10	C3	250	100	pF

NOTES:

(1) ALL RESISTORS ARE ¼ WATT, 5% TOLERANCE

(2) CAPACITORS NOTED WITH
* ARE 10% TOLERANCE
** ARE 5% TOLERANCE

(3) FOR 24 KBS DATA RATE, REPLACE 74H73 WITH JUMPER PLUG

NO.	DESCRIPTION	DATE	APP'D.
1	CHANGED R7, R8 FROM 2.0K TO 10K FOR 9.6 KBS RATE 9.1 K TO 4.7K FOR 24 KBS RATE	7-25-73	DCWW

REVISIONS

RF1013-07
